IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Kevin B. Leigh et al.	§	Group Art Unit: 2112
Serial No.: 09/872,600	§	Examiner: HUYNH, KIM T
Filed: June 1, 2001	§	
For: SYSTEM AND METHOD OF AUTOMATICALLY SWITCHING CONTROL OF A BUS IN A PROCESSOR-BASED DEVICE	§	Atty. Docket: COMP:0213/FLE (200301919-1)

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April 13, 2006 — Date

David — David M. Hoffman

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Commissioner for Patents
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Alexandria, VA 22313

Sir:

APPEAL BRIEF PURSUANT TO 37 C.F.R. §§ 41.31 AND 41.37

In accordance with M.P.E.P. § 1204.01, Appellants respectfully request to reinstate the previously-filed Appeal to the Board of Patent Appeals and Interferences for the present application. As such, this new Appeal Brief is being filed concurrently with a new Notice of Appeal. Appellants respectfully request that the fees paid for the previously filed Notice of Appeal and Appeal Brief be applied to this new Appeal. Accordingly, no fees are believed to be due. However, if any fees are due, the Commissioner is authorized to charge any additional fees which may be necessary to advance prosecution of the present application, to Account No. 08-2025, Order No. 200301919-1/FLE (COMP:0213).

1. REAL PARTY IN INTEREST

The real party in interest is Hewlett-Packard Development Company, L.P., a Texas Limited Partnership having its principal place of business in Houston, Texas and the Assignee of the above-referenced application. The Assignee of the above-referenced application will be directly affected by the Board's decision in the pending appeal.

2. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any other appeals or interferences related to this Appeal. The undersigned is Appellants' legal representative in this Appeal.

3. STATUS OF CLAIMS

Claims 1-55 are currently pending, are currently under final rejection and, thus, are the subject of this appeal.

4. STATUS OF AMENDMENTS

No claims have been amended since the final rejection. As such, there are no outstanding amendments to be considered by the Board.

5. SUMMARY OF CLAIMED SUBJECT MATTER

The present application is directed to a system and method of automatically switching control of a bus in a processor-based device. Page 2, lines 7-8. While certain system motherboards may include a controller for controlling devices on a bus, such as a SCSI controller for controlling SCSI devices, many end-users may desire incorporation of alternate controller cards which provide different or additional features. Page 3, line 21 - page. 4, line

2. Accordingly, in one exemplary embodiment, when a SCSI expansion card is connected to the expansion port, a presence detect signal is automatically asserted, thereby indicating the presence of the SCSI expansion card. Pg. 10, lines 8-11. When a SCSI expansion card is not connected to the expansion port, a switch couples the locally resident controller to the SCSI back plane, thereby enabling control of the SCSI devices by the locally resident SCSI controller. Pg. 12, lines 9-11. Conversely, when the SCSI expansion card is connected to the expansion port, the presence detect signal is asserted, which causes the switch to decouple the locally resident SCSI controller from the SCSI bus segment, thereby enabling control of the bus and the SCSI devices on the bus by a controller on the SCSI expansion card. Pg. 12, lines 15-21.

With regard to the aspect of the invention set forth in independent claim 1, discussions of the recited features of claim 1 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of switching control of a bus (e.g., 50) in a processor-based device (e.g., 10). *See, e.g.,* page 8, lines 19-22; *see also* Fig. 3. The method comprises the act of electrically coupling a first bus controller (e.g., 42) to the bus. *See, e.g.,* page 7, lines 20-22. The method also includes generating a detection signal (e.g., 82) indicative of coupling of a second bus controller (e.g., 32) to the bus. *See, e.g.,* page 10 lines 5-17; *see also*, page 12, lines 15-22. The method also comprises automatically isolating the first bus controller from the bus in response to the detection signal. *See, e.g.,* page 10, lines 1-3.

With regard to the aspect of the invention set forth in independent claim 13, discussions of the recited features of claim 13 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of switching control of a bus in a processor-based device (e.g. 10), the processor-based device comprising a first bus controller (e.g., 42) and a bus disposed on a first substrate (e.g., 28), wherein the first bus controller is coupled to the bus and configured to control the bus. *See, e.g.,* page 8, lines 15-22; *see also* Fig. 3. The method comprises the act of electrically coupling a second bus controller (e.g., 32) to the bus. *See, e.g.,* page 7, lines 20-22. The method also includes detecting presence of the second bus controller. *See, e.g.,* page 10, lines 1-3. The method further includes automatically switching control of the bus from the first bus controller to the second bus controller in response to detecting the presence of the second bus controller. *See, e.g.,* page 10, lines 1-3.

With regard to the aspect of the invention set forth in independent claim 21, discussions of the recited features of claim 21 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of switching control of a bus in a low profile server (e.g., 10), the low profile server comprising a first bus controller (e.g., 42), a bus, and an isolation device (e.g., 72), wherein the first bus controller is configured to control the bus, and wherein the isolation device is configured to isolate the first bus controller from the bus. *See, e.g.,* page 8, line 15 – page 9, line 7; *see also, e.g.,* page 12, lines 7-13; *see also* Fig. 3. The method comprises the act of connecting a second bus controller (e.g., 32) to the bus to cause the isolation device to isolate the first bus controller from the bus. *See, e.g.,* page 10, lines 1-3.

With regard to the aspect of the invention set forth in independent claim 23, discussions of the recited features of claim 23 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a processor-based device (e.g., 10). *See, e.g.,* page 8, line 15 – page 9, line 7; *see also* Fig. 3. The device comprises a processor (e.g., 36) and a memory (e.g., 40) coupled to the processor. *See, e.g.,* page 8, lines 1-13. The device also comprises a first substrate (e.g., 28). The first substrate includes a bus disposed on the first substrate. *See, e.g.,* page 8, lines 1-15. The first substrate also comprises a first bus controller (e.g., 42) disposed on the first substrate, the first bus controller being coupled to the processor and to the bus. *See, e.g.,* page 8, lines 1-15. The first substrate also includes an isolation device (e.g., 72) disposed on the first substrate, the isolation device being configured to couple the first bus controller to the bus, and to automatically isolate the first bus controller from the bus in response to detection of a second bus controller (e.g., 32) coupled to the bus. *See, e.g.,* page 10, lines 1-3; *see also, e.g.*, page 12, line 15 – page 13, line 3.

With regard to the aspect of the invention set forth in independent claim 35, discussions of the recited features of claim 35 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a printed circuit board (e.g., 28) for a low profile server (e.g., 10). *See, e.g.,* page 7, lines 4-22. The board comprises a substrate (e.g., 28) and a bus disposed on the substrate. *See, e.g.,* page 8, lines 1-15. The board also includes a first bus controller (e.g., 42) disposed on the substrate, the first bus controller coupled to the bus and configured to control the bus. *See, e.g.,* page 8, lines 1-15; *see also e.g.*, page 12, line 15 –

page 13, line3. The board also includes an isolation device (e.g., 72) disposed on the substrate and configured to automatically isolate the first bus controller from the bus in response to detection of a second bus controller coupled to the bus. *See, e.g.,* page 10, lines 1-3; *see also, e.g.*, page 12, line 15 – page 13, line 3.

With regard to the aspect of the invention set forth in independent claim 44, discussions of the recited features of claim 44 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of manufacturing a device (e.g., 10) for switching control of a bus in a processor-based device. *See, e.g.,* page 8, lines 19-22; *see also* Fig. 3. The method comprises the act of providing a bus disposed on a substrate (e.g., 28). *See, e.g.,* page 7, lines 20-22. The method also includes connecting an expansion port (e.g., 55) to the bus, the expansion port being configured for connection to a second bus controller (e.g., 32). *See, e.g.,* page 12, lines 15-22. The method further comprises disposing an isolation device (e.g., 72) on the substrate, the isolation device being connected to the bus. *See, e.g.,* page 10, lines 1-3; *see also, e.g.,* page 12, lines 7-13. The method also comprises disposing a first bus controller (e.g., 42) on the substrate, the first bus controller being connected to the isolation device, the isolation device being configured to isolate the first bus controller from the bus when a second bus controller is connected to the expansion port. *See, e.g.,* page 10, lines 1-3.

With regard to the aspect of the invention set forth in independent claim 52, discussions of the recited features of claim 52 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of manufacturing an expansion card (e.g., 32)

connectable to a system controller board (e.g., 28) having a system bus controller (e.g., 42) configured to control the bus, and having an isolation device (e.g., 72). *See, e.g.,* page 8, lines 1-13 and 19-22; *see also, e.g.,* page 12, lines 7-13; *see also* Fig. 6. The method comprises the act of disposing an expansion bus controller (e.g., 42) on a substrate, the expansion bus controller being configured to control a bus. *See, e.g.,* page 8, line 19 – page 9, line 7. The method also comprises disposing a detect signal generator (e.g., 55) on the substrate. *See, e.g.,* page 12, lines 15-22; *see also* Fig. 6. The method also includes connecting the detect signal generator to the first expansion connector (e.g., 32); *see, e.g.,* page 12, lines 15-22. The method also comprises disposing a first expansion connector (e.g., 55) on the substrate, the first expansion connector connected to the expansion bus controller and the detect signal generator, wherein the first expansion connector is configured to couple with a cable (e.g., 62), the cable having a first end (e.g., 70) connectable to the first expansion connector and a second end (e.g., 66) connectable to a system controller board (e.g., 28) and wherein the detect signal generator is configured to generate a detect signal detectable at the second end of the cable when the expansion board is connected to the system board via the cable and wherein the isolation device is configured to isolate the system bus controller from the bus in response to the detect signal. *See, e.g.,* page 9, lines 9-17, page 10, lines 1-3, and page 12, lines 7-22.

With regard to the aspect of the invention set forth in independent claim 53, discussions of the recited features of claim 53 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a method of switching between a first device (e.g., 42) and a second device (e.g., 32) connectable to a communications medium in a processor-based device (e.g., 10). *See, e.g.,* page 8, lines 1-13 and 19-22; *see also, e.g.,* page 12, lines 7-13; *see also*

Fig. 6. The method comprises the act of electrically coupling a first device to the communications medium. *See id.* The method also includes generating a detection signal indicative of coupling of a second device to the communications medium. *See, e.g.,* page 9, lines 9-17, page 10, lines 1-3, and page 12, lines 7-22. The method also comprises automatically isolating the first device from the communications medium in response to the detection signal. *See id.*

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

First Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's first ground of rejection in which the Examiner rejected claims 1-10, 12-21, 23-31, 35-41, 43-50, and 52-55 under 35 U.S.C. § 103(a) as being unpatentable over Vivio (U.S. Patent No. 5,706,447 hereafter "the Vivio reference") in view of Alexander (U.S. Patent No. 6,701, 402, hereafter the "Alexander reference).

Second Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's second ground of rejection in which the Examiner rejected claims 11, 22, and 34 under 35 U.S.C. § 103(a) as being unpatentable over the Vivio reference in view of Alexander and in further view of Applicant Admitted Prior Art (hereafter, "AAPA").

Third Ground of Rejection for Review on Appeal:

Appellants respectfully urge the Board to review and reverse the Examiner's third ground of rejection in which the Examiner rejected claims 32-34, 42, and 51 under 35

U.S.C. § 103(a) as being unpatentable over the Vivio reference in view of the Alexander reference and in further view of Gasparik et al. (U.S. Patent No. 6,072,943, hereafter "the Gasparik reference").

7. ARGUMENT

As discussed in detail below, the Examiner has improperly rejected the pending claims. Further, the Examiner has misapplied long-standing and binding legal precedents and principles in rejecting the claims under Section 103. Accordingly, Appellants respectfully request full and favorable consideration by the Board, as Appellants strongly believe that claims 1-55 are currently in condition for allowance.

A. First Ground of Rejection

The Examiner rejected claims 1-10, 12-21, 23-31, 35-41, 43-50, and 52-55 under 35 U.S.C. § 103(a) as being unpatentable over the Vivio reference in view of the Alexander reference. Appellants respectfully traverse these rejections.

1. Judicial precedent has clearly established a legal standard for a *prima facie* obviousness rejection.

First, the burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes all of the claimed elements, but also a convincing line of reason as

to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

Second, when prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988). One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

Third, a *prima facie* case of obviousness may be rebutted by a showing that the proposed modification would render the prior art invention being modified *unsatisfactory for its intended purpose*. *In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984) (emphasis added). Furthermore, if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959); see M.P.E.P. § 2143.01.

Fourth, a *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention. *In re Geisler*, 116 F.3d 1465, 1471, 43 U.S.P.Q.2d 1362, 1366 (Fed. Cir. 1997). In fact, teaching away from the art is a *per se* demonstration of lack of *prima facie* obviousness. *In re Dow Chemical Co.*, 837 F.2d 469, 5 U.S.P.Q.2d 1529 (Fed. Cir. 1988). Accordingly, it is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 U.S.P.Q. 769, 779 (Fed. Cir. 1983); M.P.E.P. § 2145.

2. **The Examiner's rejection of independent claims 1, 21, 23, 35, 44, 52, and 53 is improper because the rejection fails to establish a *prima facie* case of obviousness.**

In rejecting independent claims 1, 21, 23, 35, 44, 52, and 53, the Examiner alleged that the Vivio reference in combination with the Alexander reference discloses all of the recited features of these claims. *See* Final Office Action mailed January 24, 2006, page 2. Appellants respectfully traverse this allegation.

As discussed above, the present application discloses a system and method of automatically switching control of a bus in a processor-based device. Page 2, lines 7-8. In one exemplary embodiment, to enable a user to install an alternative controller on an expansion card via an I/O port, a locally resident bus controller is coupled to a switch/terminator module to automatically switch control of the bus and the devices on the bus from the locally resident bus controller to a bus controller on an expansion card whenever an expansion card is connected to the expansion port. Page 8, line 20 - page 9, line 4. When an expansion card is connected to the system motherboard, the locally resident bus controller

is isolated from the bus such that a controller on the expansion card can assume control of the bus and the devices on the bus. Page 10, lines 1-3.

As described above, independent claims 1, 21, 23, 35, 44, 52, and 53 of the present application recite a method or device for automatically isolating a first bus controller from the bus in response to a second bus controller being coupled to the bus (or in response to the generation of a detection signal indicating that a second controller has been coupled to the bus). Based on the similarity of the Examiner's rejections with respect to each of the independent claims, claims 1, 21, 23, 35, 44, 52, and 53 will be discussed together. While the specific recitations may vary with regard to one or more specific independent claims, the discussion below is applicable to each of these claims.

As the Examiner acknowledged in the Final Office Action mailed January 24, 2006, the Vivio reference clearly does not disclose isolating a first bus controller from the bus, as recited in the pending claims. *See* Final Office Action, page 2. Rather, the Vivio reference is directed towards a system that facilitates the addition or removal of an additional processor to a computer system. *See* Vivio, col. 8, lines 50-62; *see also*, Fig. 5. This second processor is *intended to work in conjunction* with the first processor and *not* to take independent control of the bus 120. *See id.*

Contrary to the Examiner's assertion, however, the Alexander reference does not cure this deficiency in the Vivio reference. The Alexander reference discloses a system for selectively operating a host device controller in a first mode or a second mode. *See* Alexander, abstract. More specifically, the Alexander reference discloses a PLD 120 that is

configured to detect when a controller 107 is given master access to a PCI bus 115 and to disconnect the ID select line ("IDSEL") 135 from the PCI bus 115 in response to this detection. *See* Alexander, col. 3, lines 6-52. However, as described further below, the Alexander reference discloses neither "automatically isolating the first bus controller from the bus" nor performing this action "in response to the detection signal," as recited in claim 1, for example.

First, the Alexander reference clearly does not disclose "automatically isolating the first bus controller from the bus." In the Final Office Action, the Examiner alleges that when the controller 107 from the Alexander reference is coupled to the PCI bus 115, the "other masters" are automatically isolated from the PCI bus. *See* Final Office Action, page 14. Appellants, however, respectfully assert that the Examiner has misinterpreted this section of the Alexander reference. Considered in its entirety (see MPEP 2141.02 stating that prior art must be considered in its entirety, including disclosures that teach away from the claims), the section of the Alexander reference cited by the Examiner states:

> When controller 107 is given master access to PCI bus 115, controller 107 is the only master communicating with disk controller 110 (i.e., controller 107 is provided with sole access to disk controller 110). Accordingly, other masters connected to PCI bus 115 may not communicate with disk controller 110 until controller 107 relinquishes master access to PCI bus 115.

Alexander, col. 3, lines 7-13.

Thus, Alexander discloses granting controller 107 master access to the PCI bus. However, contrary to the Examiner's allegations, such master access is not disclosed to isolate the "other masters" from the PCI bus 115. *Id.* Rather, the "other masters" although deprived of their control of the PCI bus 115, appear to remain in contact and in

communication with other devices on the PCI bus 115 *besides* the disk controller 110. *See id.* In other words, the other masters are never isolated from the PCI bus 115. *See id.* Rather, they merely lose control of the PCI bus 115 and contact with the disk controller 110. *See id.* More specifically, slightly before the section of the Alexander reference cited by the Examiner, it is explained that master access to the PCI bus is provided by an arbitration circuit that is configured to designate which device has master access. Alexander, col. 3, lines 3-5. This arbitration circuit obviates the need *to isolate* "other masters" by enabling a plurality of masters *to share control* of the PCI bus 115 by giving each master control of the PCI bus 115 for a certain amount of time. *See id.*; *see also* col. 3, lines 37-51 (stating that "another master may gain master access" and referring to "other devices that may become master of the PCI bus 115" without any discussion of either isolating or disconnecting other potential masters). As such, as stated above, when a particular master is not in control of the PCI bus 115, *it is not isolated; it is merely not in control. See* Alexander, col. 3, lines 43-51 (explaining that another master may gain control of the PCI bus 115 after the controller 107, but the controller 107 *remains in contact* with the disk controller 110 over the PCI bus 115). For at least this reason, Appellants respectfully assert that the Vivio reference and the Alexander reference, taken alone or in combination, fail to disclose the above-recited claim features.

Second, the above-described grant of control to the controller 107 is also not performed "in response to the detection signal," as further recited in claim 1, for example. More specifically, the controller 107 is never described in the Alexander reference as being coupled or connected to the PCI bus 115. Rather, the controller 107 is described initially and consistently as being an *integral part of the circuit 100. See* Alexander, col. 2, lines 58-67.

As such, the Alexander reference does not disclose any type of detection signal that would accompany the coupling of the controller 107 to the PCI bus 115. Accordingly, the Alexander reference clearly cannot disclose taking action in response to a detection signal, because the Alexander reference does not disclose a detection signal. For this additional reason, Appellants respectfully assert that the Vivio reference and the Alexander reference, taken alone or in combination, fail to disclose the above-recited claim features.

For at least the reasons set forth above, Appellants respectfully assert that the Examiner has not established a *prima facie* case of obviousness against independent claims 1, 21, 23, 35, 44, 52, and 53. Accordingly, Appellants respectfully request that the Board overturn the rejection and allow independent claims 1, 21, 23, 35, 44, 52, and 53, and the claims that depend therefrom.

3. **The Examiner's rejection of independent claim 13 is improper because the rejection fails to establish a *prima facie* case of obviousness.**

Appellants also respectfully assert that the cited references, taken alone or in combination, do not disclose several features of independent claim 13. For example, independent claim 13 recites "automatically switching control of the bus from the first bus controller to the second bus controller *in response to detecting the presence of the second bus controller*." (Emphasis added). The Examiner conceded in the Office Action that the Vivio reference does not disclose this feature and relied on the Alexander reference to disclose this feature. *See* Office Action, page 2. Appellants respectfully assert, however, that the Alexander reference does not cure this deficiency in the Vivio reference. As described above, there is no discussion in the Alexander reference of detecting the presence of a second

bus controller, much less of switching control of the PCI bus 115 *in response* to detecting the presence of the second bus controller, as recited in claim 13. For at least this reason, Appellants respectfully assert that claim 13 and the claims that depend therefrom are patentable in view of the cited references taken alone or in combination.

For at least the reasons set forth above, Appellants respectfully assert that the Examiner has not established a *prima facie* case of obviousness against independent claim 13. Accordingly, Appellants respectfully request that the Board overturn the rejection and allow independent claim 13 and the claims that depend therefrom.

4. **The Examiner's rejection of independent claim 1, 13, 21, 23, 35, 44, 52, and 53 is improper because the proposed combination would make the Vivio reference unsuitable for its intended purpose.**

Furthermore, as described above, a *prima facie* case of obviousness may be rebutted by a showing that the proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose. *In re Gordon*, 221 U.S.P.Q. 1125 (Fed. Cir. 1984). See MPEP 2143.01. In this case, Appellants respectfully assert that it is improper to modify the Vivio reference in view of the Alexander reference, because the very idea of switching control from one bus to another is antithetical to the intended purpose of the Vivio reference.

As described above, the Vivio reference is directed towards a system that facilitates the addition of a second processor to a computer system. *See* Vivio, col. 8, lines 50-62; *see also*, Fig. 5. This second processor is *intended to work in conjunction* with the first processor

and *not* to take control of the bus 120. *See id.* The Examiner proposes to modify the Vivio reference such that the insertion of the processor 128 disconnects the processor 122 from the PCI bus 120. This modification, however, would defeat the entire purpose of the system disclosed in the Vivio reference - leveraging the computing power of *dual processors* (if desired). *See* Vivio, abstract and col. 5, lines 34-41. In other words, modifying the Vivio system as proposed by the Examiner would convert the Vivio system from a multi-processor system to a single processor system. As such, any attempt to modify the Vivio reference to support switching control of PCI bus 120 and/or isolating the processor 122 would clearly make the system disclosed in the Vivio reference unsatisfactory for its intended purpose which is use in a multi-processor system. *See* Vivio, title and col. 5, lines 34-40.

For this additional reason, Appellants respectfully assert that the combination of the Vivio reference and the Alexander reference is improper. Accordingly, Appellants respectfully request that the Board overturn the rejection and allow independent claims 1, 13, 21, 23, 35, 44, 52, and 53, and the claims that depend therefrom.

5. **The Examiner's rejection of independent claim 1, 13, 21, 23, 35, 44, 52, and 53 is improper because the proposed combination would change the principle of operation of the Vivio reference.**

In addition, as described above, a *prima facie* case of obviousness may also be rebutted by a showing that the proposed modification would change the principle of operation of the prior art invention being modified. *In re Ratti*, 270 F.2d 810, 123 U.S.P.Q. 349 (C.C.P.A. 1959). In this case, Appellants respectfully assert that it is improper to modify the Vivio reference in view of the Alexander reference, because the principle of operation of the

Vivio reference is the facilitation of operation with either a single processor 122 or with dual processors 122 and 128. *See* Figs. 2-4. Modifying the Vivio reference as suggested by the Examiner, however, would prevent the system disclosed in the Vivio reference from ever operating with dual processors, because the insertion of the second processor 128 would *automatically isolate* the first processor 122 from the system. In other words, as described above, modifying the Vivio system as proposed by the Examiner would convert the Vivio system from a multi-processor system to a single processor system. Such a drastic change in operation would clearly constitute a change in the operating principle of the Vivio reference and render it unsuitable for its intended purpose.

For at least this additional reason, Appellants respectfully assert that the combination of the Vivio reference and the Alexander reference is improper. Accordingly, Appellants respectfully request that the Board overturn the rejection and allow independent claims 1, 13, 21, 23, 35, 44, 52, and 53, and the claims that depend therefrom.

6. **The Examiner's rejection of independent claim 1, 13, 21, 23, 35, 44, 52, and 53 is improper because the Vivio reference teaches away from the claimed invention.**

Lastly, a *prima facie* case of obviousness may also be rebutted by showing that the art, in any material respect, teaches away from the claimed invention. *In re Geisler*, 43 U.S.P.Q.2d at 1366 (Fed. Cir. 1997). In this case, Appellants respectfully assert that the Vivio reference clearly teaches away from the claimed invention. Specifically, as described above, Appellants note that the Vivio reference teaches a computer system 100 including a multi-*processor* bus 120. Vivio, title and col. 5, lines 34-40. This multi-processor system is

intended to accommodate "one or more P6 processors." Vivio, col. 6, lines 22-24. These one or more P6 processors are clearly intended to share the processor bus 120. Such dual processor function advantageously increases the functionality and performance of the computer system 100. *See* Vivio, col. 5, lines 2-8. As such, the Vivio reference teaches the desirability of employing dual processors. *See* Vivio, col. 5, lines 34-41; *see also* Figs. 2-5. In fact, as described above, the entire purpose of the invention claimed in the Vivio reference is to facilitate dual processor operation. *See* Vivio, col. 4, lines 1-17. On the contrary, claim 1, for example, recites isolating a first bus controller in response to a second bus controller being coupled to the bus – thereby preventing dual controller operation of the bus. Accordingly, Appellants respectfully assert that the Vivio reference clearly teaches away from a modification that would effectively eliminate its multi-processor functionality.

For this additional reason, Appellants respectfully assert that the combination of the Vivio reference and the Alexander reference is improper. Accordingly, Appellants respectfully request that the Board overturn the rejection and allow independent claims 1, 13, 21, 23, 35, 44, 52, and 53, and the claims that depend therefrom.

B. Second and Third Grounds of Rejection

1. The Examiner's rejection of independent claims 11, 22, and 34 is improper because the rejection fails to establish a prima facie case of obviousness.

The Examiner rejected claims 11, 22, and 34 under 35 U.S.C. § 103(a) as being unpatentable over the Vivio reference in view of the Alexander reference in further view of Applicant's Admitted Prior Art ("AAPA"). Appellants respectfully traverse these rejections.

Claims 11, 22, and 34 depend from independent claims 1, 21, and 23, respectively, each of which is discussed above. Moreover, each of the Examiner's obviousness rejections is based primarily on the Vivio and Alexander references, which are discussed above. With this in mind, Appellants respectfully assert that the Applicant's Admitted Prior Art employed in conjunction with the Vivio and Alexander references, does not obviate the deficiencies of the Vivio and Alexander references as discussed in the foregoing remarks regarding the Examiner's rejections of independent claims 1, 21, and 23. Accordingly, Appellants respectfully assert that claims 11, 22, and 34 are not only patentable for their dependencies on allowable base claims but also by virtue of the additional features recited therein.

In light of the forgoing remarks, Appellants respectfully request that the Board withdraw the obviousness rejections of claims 11, 22, and 34. Additionally, Appellants respectfully request that the Board direct the Examiner to allow these claims.

2. **The Examiner's rejection of independent claims 32-34, 42, and 51 is improper because the rejection fails to establish a prima facie case of obviousness.**

The Examiner rejected claims 32-34, 42, and 51 under 35 U.S.C. § 103(a) as being unpatentable over the Vivio reference in view of the Alexander reference in further view of the Gasparik reference. Appellants respectfully traverse these rejections.

Claims 32-34, 42, and 51 depend from independent claims 23, 35, and 44, respectively, each of which is discussed above. Moreover, each of the Examiner's obviousness rejections is based primarily on the Vivio and Alexander references, which are

discussed above. With this in mind, Appellants respectfully assert that the Gasparik reference employed in conjunction with the Vivio and Alexander references does not obviate the deficiencies of the Vivio and Alexander references as discussed in the foregoing remarks regarding the Examiner's rejections of independent claims 23, 35, and 44. Accordingly, Appellants respectfully assert that claims 32-34, 42, and 51 are not only patentable for their dependencies on allowable base claims but also by virtue of the additional features recited therein.

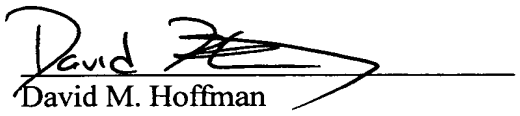
In light of the forgoing remarks, Appellants respectfully request that the Board withdraw the obviousness rejections in relation to claims 32-34, 42, and 51. Additionally, Appellants respectfully request that the Board direct the Examiner to allow these claims.

Conclusion

Appellants respectfully submit that all pending claims are in condition for allowance. However, if the Examiner or Board wishes to resolve any other issues by way of a telephone conference, the Examiner or Board is kindly invited to contact the undersigned attorney at the telephone number indicated below.

Respectfully submitted,

Date: April 13, 2006



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8. APPENDIX OF CLAIMS ON APPEAL

Listing of Claims:

1. A method of switching control of a bus in a processor-based device, the method comprising the acts of:

electrically coupling a first bus controller to the bus;

generating a detection signal indicative of coupling of a second bus controller to the bus; and

automatically isolating the first bus controller from the bus in response to the detection signal.

2. The method as recited in claim 1, comprising the act of terminating the first bus controller.

3. The method as recited in claim 2, wherein the first bus controller is terminated in response to detection of the detection signal.

4. The method as recited in claim 1, wherein the bus comprises a plurality of traces disposed on a substrate, wherein the first bus controller is electrically coupled to a first segment of the plurality of traces, and wherein the second bus controller is electrically coupled to a second segment of the plurality of traces.

5. The method as recited in claim 4, comprising the act of terminating the second segment of the plurality of traces.

6. The method as recited in claim 5, comprising the act of electrically removing termination of the second segment of the plurality of traces in response to detection of the second bus controller.

7. The method as recited in claim 1, wherein the first bus controller is disposed on a first substrate, and the second controller is disposed on a second substrate, the second substrate being coupled to the first substrate, and wherein the act of generating a detection signal comprises the act of transmitting the detection signal from the second substrate to the first substrate.

8. The method as recited in claim 7, wherein the first substrate comprises an expansion port, and a first end of the cable is connected to the expansion port.

9. The method as recited in claim 1, wherein the bus comprises a SCSI bus.

10. The method as recited in claim 7, wherein the first substrate and the second substrate each comprise a printed circuit board.

11. The method as recited in claim 7, wherein the first substrate and the second substrate are disposed within a low profile server.

12. The method as recited in claim 1, wherein the act of electrically coupling comprises the act of coupling the first bus controller to the bus using a switch.

13. A method of switching control of a bus in a processor-based device, the processor-based device comprising a first bus controller and a bus disposed on a first substrate, wherein the first bus controller is coupled to the bus and configured to control the bus, the method comprising the acts of:

electrically coupling a second bus controller to the bus;

detecting presence of the second bus controller; and

automatically switching control of the bus from the first bus controller to the second bus controller in response to detecting the presence of the second bus controller.

14. The method as recited in claim 13, wherein the act of detecting the presence of the second bus controller comprises the act of generating a detect signal when the second bus controller is electrically coupled to the bus.

15. The method as recited in claim 13, wherein the act of automatically switching control of the bus comprises the acts of:

isolating the first bus controller from the bus; and

terminating the isolated first bus controller.

16. The method as recited in claim 13, comprising the act of terminating the bus proximate the first bus controller.

17. The method as recited in claim 14, wherein the bus is terminated proximate the first bus controller in response to detecting the presence of the second bus controller.

18. The method as recited in claim 15, wherein the second bus controller is disposed on a second substrate coupled to the first substrate.

19. The method as recited in claim 18, wherein the first substrate comprises an expansion port, and the method comprises the act of terminating the bus proximate the expansion port.

20. The method as recited in claim 19, comprising the act of removing termination of the bus proximate the expansion port in response to detecting the presence of the second bus controller.

21. A method of switching control of a bus in a low profile server, the low profile server comprising a first bus controller, a bus, and an isolation device, wherein the first bus controller is configured to control the bus, and wherein the isolation device is configured to isolate the first bus controller from the bus, the method comprising the act of:

connecting a second bus controller to the bus to cause the isolation device to isolate the first bus controller from the bus.

22. The method as recited in claim 21, wherein the first bus controller is disposed on a first substrate, and wherein the second bus controller is disposed on a second substrate, and the act of connecting the second bus controller to the bus comprises the acts of:

disposing a cable in the low profile server, the cable comprising a first end and a second end;

connecting the first end of the cable to the first substrate; and

connecting the second end of the cable to the second substrate.

23. A processor-based device, comprising:

a processor;

a memory coupled to the processor; and

a first substrate, comprising:

a bus disposed on the first substrate;

a first bus controller disposed on the first substrate, the first bus controller being coupled to the processor and to the bus; and

an isolation device disposed on the first substrate, the isolation device being configured to couple the first bus controller to the bus, and to automatically isolate the first bus controller from the bus in response to detection of a second bus controller coupled to the bus.

24. The device as recited in claim 23, comprising an expansion port disposed on the first substrate and coupled to the bus, wherein the expansion port is connectable to a second substrate, and wherein the second bus controller is disposed on the second substrate.

25. The device as recited in claim 23, wherein the second bus controller is disposed on a second substrate, and the device comprises a cable having a first end and a second end, the first end being connectable to the first substrate, and the second end being connectable to the second substrate.

26. The device as recited in claim 24, comprising a termination device disposed on the first substrate, the termination device being configured to terminate the bus proximate the expansion port when the second bus controller is not coupled to the bus.

27. The device as recited in claim 23, comprising a termination device disposed on the first substrate, the termination device being configured to terminate the bus proximate the first bus controller in response to detection of the second bus controller.

28. The device as recited in claim 23, wherein the isolation device comprises an electronic switch.

29. The device as recited in claim 28, wherein the electronic switch comprises a transistor.

30. The device as recited in claim 23, wherein the processor and the memory are disposed on the first substrate.

31. The device as recited in claim 23, wherein the bus comprises a SCSI bus.

32. The device as recited in claim 31, comprising a SCSI device connectable to the SCSI bus.

33. The device as recited in claim 32, wherein the SCSI device comprises a hard disk drive.

34. The device as recited in claim 23, wherein the device comprises a low profile server.

35. A printed circuit board for a low profile server, the system board comprising:

a substrate;

a bus disposed on the substrate;

a first bus controller disposed on the substrate, the first bus controller coupled to the bus and configured to control the bus; and

an isolation device disposed on the substrate and configured to automatically isolate the first bus controller from the bus in response to detection of a second bus controller coupled to the bus.

36. The board as recited in claim 35, comprising a termination device disposed on the substrate and configured to terminate the first bus controller in response to detection of the second bus controller coupled to the bus.

37. The board as recited in claim 35, comprising an expansion port disposed on the substrate and coupled to the bus, wherein the second bus controller is coupled to the bus via the expansion port.

38. The board as recited in claim 37, comprising a termination device disposed on the substrate and configured to terminate the bus proximate the expansion port when the second bus controller is not coupled to the bus via the expansion port.

39. The board as recited in claim 35, wherein the isolation device comprises an electronic switch.

40. The board as recited in claim 39, wherein the electronic switch comprises a transistor.

41. The printed circuit board as recited in claim 35, comprising:

a memory disposed on the substrate; and

a processor disposed on the substrate, the processor being coupled to the memory and to the first bus controller.

42. The printed circuit board as recited in claim 35, wherein a SCSI device is coupled to the bus, the SCSI device being controllable by the first bus controller or the second bus controller.

43. The printed circuit board as recited in claim 42, wherein the SCSI device comprises a hard disk drive.

44. A method of manufacturing a device for switching control of a bus in a processor-based device, the method comprising the acts of:

providing a bus disposed on a substrate;

connecting an expansion port to the bus, the expansion port being configured for connection to a second bus controller;

disposing an isolation device on the substrate, the isolation device being connected to the bus; and

disposing a first bus controller on the substrate, the first bus controller being connected to the isolation device, the isolation device being configured to

isolate the first bus controller from the bus when a second bus controller is connected to the expansion port.

45. The method as recited in claim 44, comprising the act of:

disposing a termination device on the substrate, the termination device being connected to the bus.

46. The method as recited in claim 45, wherein the termination device is connected to the bus proximate the first bus controller.

47. The method as recited in claim 46, wherein the termination device is configured to terminate the first bus controller when the second bus controller is connected to the expansion port.

48. The method as recited in claim 45, wherein the termination device is connected to the bus proximate the expansion port.

49. The method as recited in claim 48, wherein the termination device is configured to terminate the bus proximate the expansion port when the second bus controller is not connected to the expansion port.

50. The method as recited in claim 44, wherein the bus comprises a SCSI bus.

51. The method as recited in claim 44, wherein the first bus controller comprises a SCSI bus controller.

52. (previously presented) A method of manufacturing an expansion card connectable to a system controller board having a system bus controller configured to control the bus, and having an isolation device, the method comprising the acts of:

disposing an expansion bus controller on a substrate, the expansion bus controller being configured to control a bus;

disposing a detect signal generator on the substrate;

connecting the detect signal generator to the first expansion connector; and

disposing a first expansion connector on the substrate, the first expansion connector connected to the expansion bus controller and the detect signal generator,

wherein the first expansion connector is configured to couple with a cable, the cable having a first end connectable to the first expansion connector and a second end connectable to a system controller board, ~~and~~

wherein the detect signal generator is configured to generate a detect signal detectable at the second end of the cable when the expansion board is connected to the system board via the cable, and

wherein the isolation device is configured to isolate the system bus controller from the bus in response to the detect signal.

53. A method of switching between a first device and a second device connectable to a communications medium in a processor-based device, the method comprising the acts of:

electrically coupling a first device to the communications medium;

generating a detection signal indicative of coupling of a second device to the communications medium; and

automatically isolating the first device from the communications medium in response to the detection signal.

54. The method as recited in claim 53, wherein the communications medium comprises a point-to-point interconnect.

55. The method as recited in claim 53, wherein the communications medium comprises shared bus.

9. **EVIDENCE APPENDIX**

None

10. **RELATED PROCEEDING APPENDIX**

None